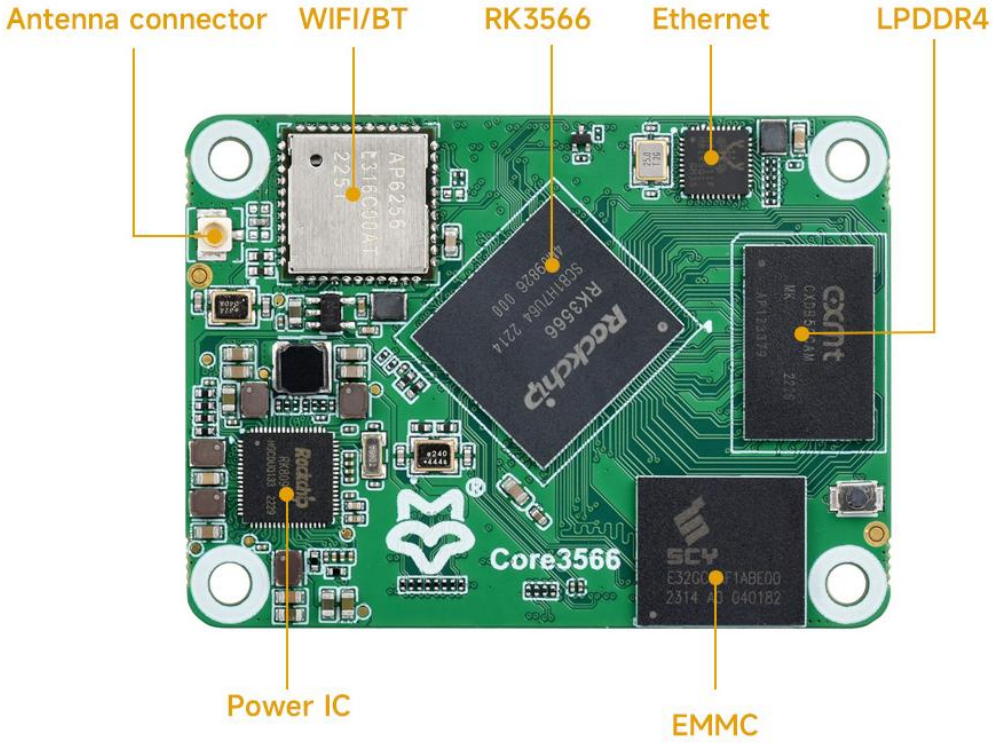
Chapter 1. Introduction

1.1. Introduction



Core3566 highly integrates the function of Rockchip RK3566 quad-core processor in a compact board. RK3566 integrates quad-core A55 CPU, dual-core ARM G52 GPU, VPU, NPU, supports video output, PCIE, CSI and other interfaces, and is very suitable for For embedded applications, different RAM, eMMC flash memory specifications and wireless module specifications are available.

o **NOTE**

Unless otherwise stated, for this document Core3566 also refers to Core3566 Lite.

1.2. Features

Key features of the Core3566 are as follows:

- Rockchip RK3566, quad core Cortex-A55 (ARM v8) 64-bit SoC @ 1.8GHz with Arm Mali-G52 EE GPU, 0.8 TOPS NPU
- Small Footprint 55mm × 40mm × 4.7mm module
  - 4 × M2.5 mounting holes
- H.265 (HEVC) (upto 4Kp60 decode), H.264 (upto 1080p60 decode, 1080p30 encode)
- OpenGL ES 1.1/2.0/3.2，OpenCL 2.0，Vulkan 1.1
- Options for 2GB/4GB LPDDR4-3700 SDRAM with ECC

- Options for 0GB (Core3566 Lite), 32GB eMMC flash memory (see Appendix B)
  - Peak eMMC bandwidth 400MBps (the speed supported by the hardware)
- Option for certified radio module with:
  - 2.4 GHz, 5.0 GHz IEEE 802.11 b/g/n/ac wireless
  - Bluetooth 5.0, BLE
- Gigabit Ethernet PHY supporting IEEE 802.3
- 1 × PCIe 1-lane Host, Gen 2
- 1 × USB 2.0 port (high speed)
- 28 × GPIO supporting either 1.8V or 3.3V signalling and peripheral options:
  - Up to 5 × UART
  - Up to 2 × I2C
  - Up to 2 × SPI
  - Up to 6× PWM channels
- 1 × HDMI 2.0 ports (up to 4Kp60 supported)
- MIPI DSI:
  - 1× 2-lane MIPI DSI display port
  - 1× 4-lane MIPI DSI display port
- MIPI CSI:
  - 2× 2-lane MIPI CSI display port
- Single +5V PSU input.

Chapter 2. Interfaces

2.1. Wireless

The Core3566 can be supplied with an on-board wireless module based on the AMPAK AP6256 supporting both:

- 2.4 GHz, 5.0 GHz IEEE 802.11 b/g/n/ac wireless
- Bluetooth 5.0, BLE

Alternatively there is a standard U.FL connector on the module, so that an external antenna can be used.

Q WARNING

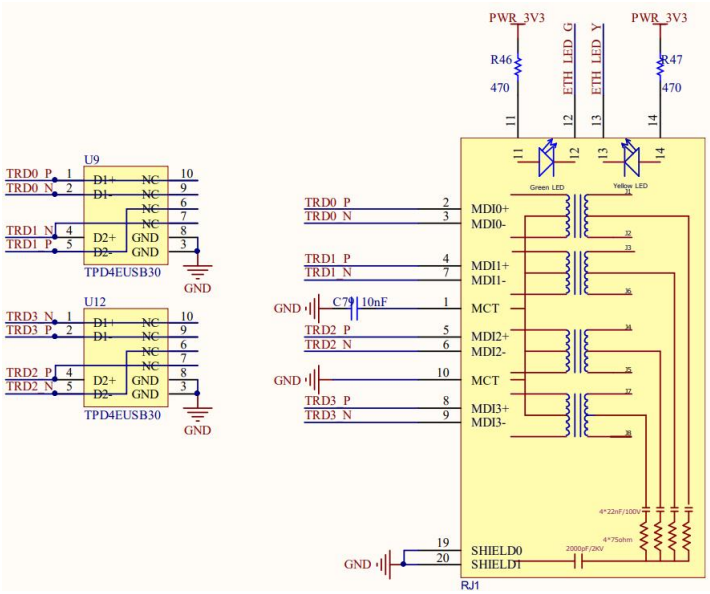
Not connecting an external antenna will affect the WiFi signal.

2.2. Ethernet

The Core3566 has an on-board Gigabit Ethernet PHY — RTL8211F — some of the major features of this PHY include;

- Meets or Exceeds EEE802.3ab standards for 1000Base-T
- High performance for EMI suppression, Crosstalk, Return Loss and Consistent Electrical
- Minimum 1500Vrms isolation per IEEE802.3 requirement

A standard 1:1 RJ45 MagJack is all that is necessary to provide an Ethernet connection to the Core3566 Typical wiring of a MagJack supporting PoE, and with added ESD protection.



2.3. PCIe (Gen2 x1)

The Core3566 has an internal PCIe 2.0 x1 host controller. PCIe is the abbreviation of PCI-Express. RK3566 supports PCIe V2.1 protocol and has the following characteristics:

- Compatible with Gen1/Gen2
- Only supports Root Complex (RC) working mode
- Support x1 mode, with 1 pair of TX/RX differential signal pair
- A single data channel can support a maximum signal transmission rate of 5GT/s, and the codec adopts 8b/10b mode
- Full duplex mode;
- Support spread spectrum function

On the Core3566 the product designer is free to choose how the interface is used.

Q WARNING

You should ensure that there is a suitable OS driver for any host controller that is chosen before proceeding to a prototype.

Connecting a PCIe device follows the standard PCIe convention. The Core3566 has on-board AC coupling capacitors for CLK and PCIe_TX signals. However the PCIe_RX signals need external coupling capacitors close to the driving source (the device TX), if you are using an external PCIe/NVMe card these capacitors will be on-board. The PCIe convention is that if you are wiring directly to an IC then the TX and RX pairs need to be swapped (i.e. TX → RX, RX → TX). If you are wiring to a connector then this is typically labelled from the host point of view and so TX/RX swaps aren't required. Additionally the PCIe_CLK_nREQ must be connected to ensure the Core3566 produces a clock signal, and the PCIe_nRST should also be connected to ensure the device is correctly reset when required.

The differential PCIe signals should be routed as 90Q differential pairs, with suitable clearances. There is no need to match the lengths between pairs, only the signals within a Pair need to be length matched ideally to better than 0.1mm.

2.4. USB 2.0 (high speed)

The USB 2.0 interface supports up to 480Mbps signalling. The differential pair should be routed as a 90Q differential pair. The length of the P/N signals should ideally be matched to better than 0.15mm.

o NOTE

The port is capable of being used as a true USB On-The-Go (OTG) port. The USB_OTG_ID pin is used to select between USB host and device that is typically wired to the ID pin of a Micro USB connector. If used as a host, connect the USB_OTG_ID pin to ground.

2.5. GPIO

There are 28 pins available for general purpose I/O (GPIO).These pins have access to internal peripherals: I2C, PWM, SPI, and UART. GPIO14 and GPIO15 are the debug serial ports of Core3566 by default.

The RK3566 GPIO bank is powered by GPIO_VREF, this can either be connected to +1.8V for 1.8V signalling GPIO, or +3.3V for 3.3V signalling. GPIO_VREF voltage must be consistent with DTS description.

2.5.1. Alternative function assignments

Up to six alternative functions are available. The RK3566 ARM peripherals book describes these features in detail. The table below gives a quick overview.

GPIO	Num	Pull	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5
GPIO0	110	Low	SDA3	GPIO3_B6			I2C3_SDA_M1	PWM11_IR_M0
GPIO1	109	Low	SCL3	GPIO3_B5			I2C3_SCL_M1	PWM10_M0
GPIO2	108	Low	SDA5	GPIO3_B4			I2C5_SDA_M0	
GPIO3	107	Low	SCL5	GPIO3_B3			I2C5_SCL_M0	
GPIO4	111	Low	-	GPIO3_B7	PWM12_M0		UART3_TX_M1	
GPIO5	112	Low	-	GPIO3_C0	PWM13_M0		UART3_RX_M1	
GPIO6	148	Low	-	GPIO4_C4				I2S3_LRCK_M1
GPIO7	101	Low	CE1	GPIO3_A5			I2S3_SDO_M0	
GPIO8	100	Low	CE0	GPIO3_A4			I2S3_LRCK_M0	
GPIO9	114	Low	MISO	GPIO3_C2		SPI1_MISO_M1	UART5_TX_M1	I2S1_SDO3_M2
GPIO10	113	Low	MOSI	GPIO3_C1		SPI1_MOSI_M1		I2S1_SDO2_M2
GPIO11	115	Low	SCLK	GPIO3_C3		SPI1_CLK_M1	UART5_RX_M1	I2S1_SCLK_RX_M2
GPIO12	106	Low	-	GPIO3_B2			UART4_TX_M1	PWM9_M0
GPIO13	105	Low	-	GPIO3_B1			UART4_RX_M1	PWM8_M0
GPIO14	25	Low	-	GPIO0_D1			UART2_TX_M0	
GPIO15	24	Low	-	GPIO0_D0			UART2_RX_M0	
GPIO16	102	Low	-	GPIO3_A6			I2S3_SDI_M0	
GPIO17	104	Low	-	GPIO3_B0				
GPIO18	150	Low	-	GPIO4_C6	PWM13_M1	SPI3_CS0_M1/I2S3_SDI_M1		UART9_RX_M1
GPIO19	149	Low	-	GPIO4_C5	PWM12_M1	SPI3_MISO_M1/I2S3_SDO_M1		UART9_TX_M1
GPIO20	147	Low	-	GPIO4_C3	PWM15_IR_M1	SPI3_MOSI_M1		I2S3_SCLK_M1
GPIO21	146	Low	-	GPIO4_C2	PWM14_M1	SPI3_CLK_M1		I2S3_MCLK_M1
GPIO22	117	Low	-	GPIO3_C5	PWM15_IR_M0			UART7_RX_M1
GPIO23	97	Low	-	GPIO3_A1		SPI1_CS0_M1		
GPIO24	98	Low	-	GPIO3_A2			I2S3_MCLK_M0	
GPIO25	99	Low	-	GPIO3_A3			I2S3_SCLK_M0	
GPIO26	103	Low	-	GPIO3_A7				
GPIO27	116	Low	-	GPIO3_C4	PWM14_M0			UART7_TX_M1

2.6. Dual HDMI 2.0

TheCore3566 supports an HDMI interface, which can drive 4K images.HDMI signals should be routed as 100Q differential pairs. Each signal within a pair should ideally be matched to better than 0.15mm. Pairs don’ t typically need any extra matching, as they only have to be matched to 25mm.

CEC is also supported; an internal 27kQ pullup resistor is included in the Core3566.

Basic on-board ESD protection is provided for the I2C EDID signals and the CEC signals; internal pullup and pulldown resistors are also provided.

2.7. CSI-2 (MIPI serial camera)

The Core3566 supports two camera ports: CSI0 (2 lanes) and CSI1 (2 lanes). CSI signals should be routed as 100Q differential pairs. Each signal within a pair should ideally be matched to better than 0.15mm.

o **NOTE**

The Core3566 official firmware supports Sony IMX219 camera sensor.

2.8. DSI (MIPI serial display)

RK3566 integrates two MIPI-DSI controllers, DSI0 (2 channels) and DSI1 (4 channels), the rate can reach 2.5Gbps/lane, and the maximum output resolution can reach 1920x1080@60Hz.

Although Linux kernel drivers are available, the DSI interface is not currently documented. Only DSI displays supported by the official Core3566 firmware are supported. DSI signals should be routed as 100Q differential pairs; each signal within a pair should ideally be matched to better than 0.15mm.

o **NOTE**

While only official DSI displays are supported, other displays can be added using the parallel DPI interface which is available as a GPIO alternative function. The Core3566 supports up to three displays of any type (HDMI, DSI, DPI) at any one time.

2.9. I2C (SDA0 SCL0)

This internal I2C bus is normally allocated to the CSI1 and DSI1, as these devices are controlled by the firmware. It can be used as a general I2C bus if the CSI1 ad DSI1 interfaces aren' t being used, or are being controlled by the firmware.

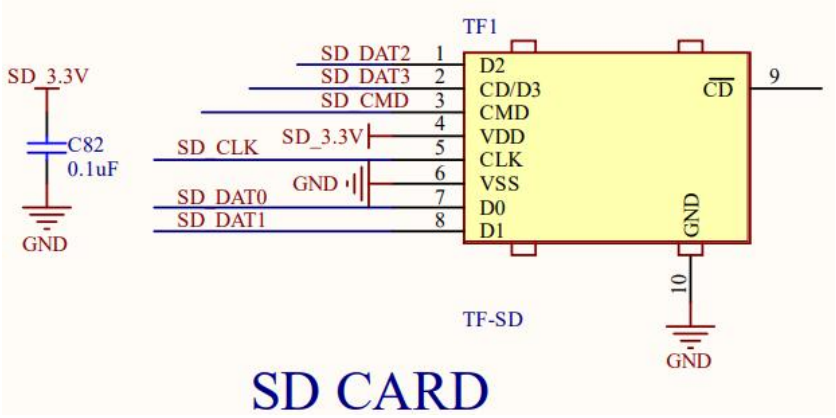
2.10. I2C (ID_SD ID_SC)

This I2C bus is normally used for identifying HATs and controlling CSI0 and DSI0 devices. If the firmware isn' t using the I2C bus e.g. CSI0 and DSI0 aren' t being used then these pins may be used as GPIO 0 and GPIO 1 if required.

2.11. SDIO/eMMC

The Core3566Lite does not have on-board eMMC. The eMMC signals are available on the connector so that an external eMMC or SD card can be used.

The SD_PWR_ON signal is used to enable an external power-switch to turn on power to the SD card,and the default is pull-up; for eMMC it typically isn’ t used. The onboard eMMC is connected to the SD card at the same time, and the SD card will be started first.



2.12. RUN_PG

This pin when high signals that the Core3566 has started. Driving this pin low resets the module. This should be done with caution.

2.13. eMMC_D0

In the case of not connecting the SD card, press the button and pull it down before powering on, and the Core3566 will enter the MASKROM mode.

2.14. LED_nACT

This pin is designed to drive the LED to blink by default, and the user can change its state by modifying the kernel.

2.15. LED_nPWR

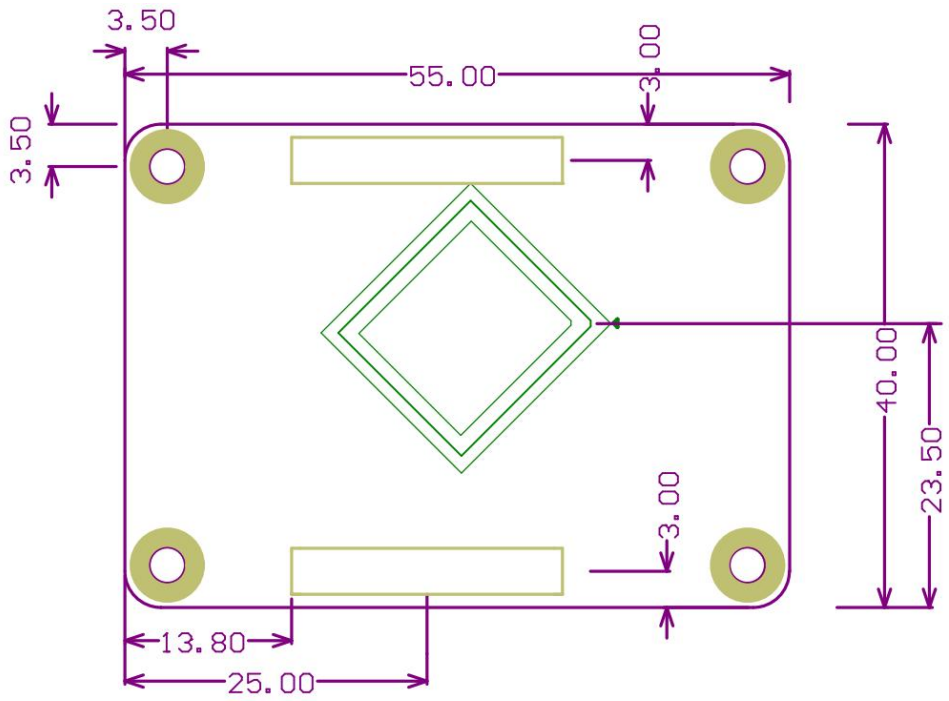
This pin needs to be buffered to drive an LED. This signal indicates the CPU power supply status.

Chapter 3. mechanical

3.1. Mechanical

The RK3566 is a compact 40mm × 55mm module. The Module is 4.7mm deep, but when connected the height will be 5.078mm or 6.578mm depending on the stacking height chosen.

1. 4 × M2.5 mounting holes (inset 3.5mm from module edge)
2. PCB thickness 1. 2mm ± 10%
3. RK3566 SoC height including solder balls 0.7 ± 0.11mm
4. Stacking height either:
    a. 1.5mm with mating connector (clearance under Core3566 0mm): DF40C-100DS-0.4v
    b. 3.0mm with mating connector (clearance under Core3566 1.5mm): DF40HC(3.0)-100DS-0.4v



Top view unit:mm

Chapter 4. Pinout

Pin	Signal	Description
1	GND	Ground (0V)
2	GND	Ground (0V)
3	Ethernet_Pair3_P	Ethernet pair 3 positive (connect to transformer or MagJack)
4	Ethernet_Pair1_P	Ethernet pair 1 positive (connect to transformer or MagJack)
5	Ethernet_Pair3_N	Ethernet pair 3 negative (connect to transformer or MagJack)
6	Ethernet_Pair1_N	Ethernet pair 1 negative (connect to transformer or MagJack)
7	GND	Ground (0V)
8	GND	Ground (0V)
9	Ethernet_Pair2_N	Ethernet pair 2 negative (connect to transformer or MagJack)
10	Ethernet_Pair0_N	Ethernet pair 0 negative (connect to transformer or MagJack)
11	Ethernet_Pair2_P	Ethernet pair 2 positive (connect to transformer or MagJack)
12	Ethernet_Pair0_P	Ethernet pair 0 positive (connect to transformer or MagJack)
13	GND	Ground (0V)
14	GND	Ground (0V)
15	Ethernet_nLED3	High = Link Up at 1000mbps Blinking = Transmitting or Receiving
16	Reserved	NC
17	Ethernet_nLED2	High = Link Up at 100mbps Blinking = Transmitting or Receiving
18	Reserved	NC
19	Reserved	NC
20	Reserved	NC
21	Pi_nLED_Activity	1U19 -- PWM6/SPI0_MISO_M0/GPIO0_C5_d
22	GND	Ground (0V)
23	GND	Ground (0V)
24	GPIO3_A7	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
25	GPIO4_C2	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
26	GPIO4_C5	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V

27	GPIO4_C3	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
28	GPIO3_B1	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
29	GPIO3_A6	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
30	GPIO4_C4	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
31	GPIO3_B2	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
32	GND	Ground (0V)
33	GND	Ground (0V)
34	GPIO3_C0	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
35	ID_SC	(1T4 -- I2C3_SCL_M1/PWM10_M0/GPIO3_B5_d) GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
36	ID_SD	(1V2 -- I2C3_SDA_M1/PWM11_IR_M0/GPIO3_B6_d) GPIO: typically a 3.3V signal, but can be a 1.8Vsignal by connecting GPIO_VREF to 1.8V
37	GPIO3_A5	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
38	GPIO3_C3	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
39	GPIO3_A4	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
40	GPIO3_C2	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
41	GPIO3_A3	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
42	GND	Ground (0V)
43	GND	Ground (0V)
44	GPIO3_C1	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
45	GPIO3_A2	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V

46	GPIO3_C5	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
47	GPIO3_A1	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
48	GPIO3_C4	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
49	GPIO4_C6	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
50	GPIO3_B0	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
51	GPIO0_D0	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
52	GND	Ground (0V)
53	GND	Ground (0V)
54	GPIO3_B7	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
55	GPIO0_D1	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
56	GPIO3_B3	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 20kΩ pull up to GPIO_VREF
57	SD_CLK	SD card clock signal
58	GPIO3_B4	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 20kΩ pull up to GPIO_VREF
59	GND	Ground (0V)
60	GND	Ground (0V)
61	SD_DAT3	SD card/eMMC Data3 signal
62	SD_CMD	SD card/eMMC Command signal
63	SD_DAT0	SD card/eMMC Data0 signal
64	Reserved	NC
65	GND	Ground (0V)
66	GND	Ground (0V)
67	SD_DAT1	SD card/eMMC Data1 signal
68	Reserved	NC
69	SD_DAT2	SD card/eMMC Data2 signal

70	Reserved	NC
71	GND	Ground (0V)
72	Reserved	NC
73	Reserved	NC
74	GND	Ground (0V)
75	SD_PWR_ON	Default pull-up,Internal 10kΩ pull up to CORE_3 .3V
76	Reserved	NC
77	+5V (Input)	4.75V-5.25V. Main power input
78	GPIO_VREF	Must be connected to CORE_3 .3V (pins 84 and 86) for 3.3V GPIO or CORE_1 .8V (pins 88 and 90) for 1.8V GPIO. This pin cannot be floating or connected to ground.
79	+5V (Input)	4.75V-5.25V. Main power input
80	SCL0	I2C clock pin (AK37 -- I2C1_SCL/MCU_JTAG_TDO/GPIO0_B3_u): typically used for Camera and Display. Please pull-up resistor to V CC for normal use.
81	+5V (Input)	4.75V-5.25V. Main power input
82	SDA0	I2C Data pin (AM38 -- I2C1_SDA/PCIE20_BUTTONRSTn/MCU_JTA G_TCK/GPIO0_B4_u): typically used for Camera and Display. Please pull-up resistor toVCC for normal use.
83	+5V (Input)	4.75V-5.25V. Main power input
84	CORE_3.3V (Output)	3.3V ± 2.5%. Power Output max 300mA per pin for a total of 600 mA. This will be powered down during power-off or GLOBAL_EN being set low
85	+5V (Input)	4.75V-5.25V. Main power input
86	CORE_3.3V (Output)	3.3V ± 2.5%. Power Output max 300mA. This will be powered dow n during power-off or GLOBAL_EN being set low
87	+5V (Input)	4.75V-5.25V. Main power input
88	CORE_1.8V (Output)	1.8V ± 2.5%. Power Output max 300mA per pin for a total of 600 mA. This will be powered down during power-off or GLOBAL_EN being set low
89	WL_nDisable	A35 -- SDMMC1_PWREN/I2C4_SDA_M1/UART8_RTSn_M0/GPIO2_ B1_d
90	CORE_1.8V (Output)	1.8V ± 2.5%. Power Output max 300mA per pin for a total of 600 mA. This will be powered down during power-off or GLOBAL_EN being set low
91	BT_nDisable	D38 -- I2S2_SCLK_RX_M0/UART6_RTSn_M0/SPI1_MOSI_M0/GPIO

		2_B7_d
92	RUN_PG	Reset pin after power on, active low
93	nRPIBOOT	Low = LOADER ModeIf there is no burning system = MASKROM Mode Internally pulled up via 10kΩ to +3.3V
94	Reserved	NC
95	PI_LED_nPWR	Low = CPU Power supply is normal High or Blinking = CPU Pow er supply is abnormal
96	Reserved	NC
97	Camera_GPIO	Typically used to shut down the camera to reduce power. Reassignin g this pin to another function isn't recommended. CORE_3.3V sign alling
98	GND	Ground (0V)
99	GLOBAL_EN	Enable Signal for external high voltage BUCK
100	nEXTRST	Reset pin after power on, active low
101	USB_OTG_ID	High = Device Mode Low = Host Mode
102	PCIe_CLK_nREQ	Input (3.3V signal) PCIe clock request pin (low to request PCI clock). Internally pulled up
103	USB_N	USB D-
104	Reserved	NC
105	USB_P	USB D+
106	Reserved	NC
107	GND	Ground (0V)
108	GND	Ground (0V)
109	PCIe_nRST	Output (+3.3V signal) PCIe reset active-low
110	PCIe_CLK_P	PCIe clock Out positive (100MHz) NB AC coupling capacitor inclu ded on Core
111	Reserved	NC
112	PCIe_CLK_N	PCIe clock Out negative (100MHz) NB AC coupling capacitor inclu ded on Core
113	GND	Ground (0V)
114	GND	Ground (0V)
115	CAM1_D0_N	Input Camera1 D0 negative
116	PCIe_RX_P	Input PCIe GEN 2 RX positive NB external AC coupling capacitor r equired
117	CAM1_D0_P	Input Camera1 D0 positive

118	PCIe_RX_N	Input PCIe GEN2 RX negative NB external AC coupling capacitor required
119	GND	Ground (0V)
120	GND	Ground (0V)
121	CAM1_D1_N	Input Camera1 D1 negative
122	PCIe_TX_P	Output PCIe GEN2 TX positive NB AC coupling capacitor included on Core
123	CAM1_D1_P	Input Camera1 D1 positive
124	PCIe_TX_N	Output PCIe GEN 2 TX positive NB AC coupling capacitor included on Core
125	GND	Ground (0V)
126	GND	Ground (0V)
127	CAM1_C_N	Input Camera1 clock negative
128	CAM0_D0_N	Input Camera0 D0 negative
129	CAM1_C_P	Input Camera1 clock positive
130	CAM0_D0_P	Input Camera0 D0 positive
131	GND	Ground (0V)
132	GND	Ground (0V)
133	CAM1_D2_N	NC / Input Camera0 D0 negative
134	CAM0_D1_N	Input Camera0 D1 negative
135	CAM1_D2_P	NC / Input Camera0 D0 positive
136	CAM0_D1_P	Input Camera0 D1 positive
137	GND	Ground (0V)
138	GND	Ground (0V)
139	CAM1_D3_N	NC / Input Camera0 D1 negative
140	CAM0_C_N	Input Camera0 clock negative
141	CAM1_D3_P	NC / Input Camera0 D1 positive
142	CAM0_C_P	Input Camera0 clock positive
143	Reserved	NC
144	GND	Ground (0V)
145	Reserved	NC
146	Reserved	NC
147	Reserved	NC

148	Reserved	NC
149	Reserved	NC
150	GND	Ground (0V)
151	HDMI0_CEC	Input HDMI0 CEC. Internally pulled up with a 27kΩ. 3.3V tolerant.
152	Reserved	NC
153	HDMI0_HOTPLUG	Input HDMI0 hotplug. Internally pulled up 10kΩ. 3.3V tolerant.
154	Reserved	NC
155	GND	Ground (0V)
156	GND	Ground (0V)
157	DSI0_D0_N	Output Display0 D0 negative
158	Reserved	NC
159	DSI0_D0_P	Output Display0 D0 positive
160	Reserved	NC
161	GND	Ground (0V)
162	GND	Ground (0V)
163	DSI0_D1_N	Output Display0 D1 negative
164	Reserved	NC
165	DSI0_D1_P	Output Display0 D1 positive
166	Reserved	NC
167	GND	Ground (0V)
168	GND	Ground (0V)
169	DSI0_C_N	Output Display0 clock negative
170	HDMI0_TX2_P	Output HDMI0 TX2 positive
171	DSI0_C_P	Output Display0 clock positive
172	HDMI0_TX2_N	Output HDMI0 TX2 negative
173	GND	Ground (0V)
174	GND	Ground (0V)
175	DSI1_D0_N	Output Display1 D0 negative
176	HDMI0_TX1_P	Output HDMI0 TX1 positive
177	DSI1_D0_P	Output Display1 D0 positive
178	HDMI0_TX1_N	Output HDMI0 TX1 negative
179	GND	Ground (0V)

180	GND	Ground (0V)
181	DSI1_D1_N	Output Display1 D1 negative
182	HDMI0_TX0_P	Output HDMI0 TX0 positive
183	DSI1_D1_P	Output Display1 D1 positive
184	HDMI0_TX0_N	Output HDMI0 TX0 negative
185	GND	Ground (0V)
186	GND	Ground (0V)
187	DSI1_C_N	Output Display1 clock negative
188	HDMI0_CLK_P	Output HDMI0 clock positive
189	DSI1_C_P	Output Display1 clock positive
190	HDMI0_CLK_N	Output HDMI0 clock negative
191	GND	Ground (0V)
192	GND	Ground (0V)
193	DSI1_D2_N	Output Display1 D2 negative
194	DSI1_D3_N	Output Display1 D3 negative
195	DSI1_D2_P	Output Display1 D2 positive
196	DSI1_D3_P	Output Display1 D3 positive
197	GND	Ground (0V)
198	GND	Ground (0V)
199	HDMI0_SDA	Bidirectional HDMI0 SDA. Internally pulled up with a 1.8kΩ. 5V tolerant.
200	HDMI0_SCL	Bidirectional HDMI0 SCL. Internally pulled up with a 1.8kΩ. 5V tolerant.

Appendix B: Availability

Support

Model	Wireless	RAM LPDDR4	eMMC Storage
Core3566102000	Yes	2GB	0GB (Lite)
Core3566102032		2GB	32GB
Core3566104000		4GB	0GB (Lite)
Core3566104032		4GB	32GB
Core3566002000	No	2GB	0GB (Lite)
Core3566002032		2GB	32GB
Core3566004000		4GB	0GB (Lite)
Core3566004032		4GB	32GB